REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Non-Final Office Action of November 17, 2005 has been received and its contents carefully reviewed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 7, 12-18 and 20-26.

By this Amendment, Applicant hereby amends claims 1-3, 5, 7-12, 14, 15, 19, 20, 22 and 23, and cancels claim 6 without prejudice or disclaimer. Accordingly, claims 1-5 and 7-26 are currently pending in the present application. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, the drawings are objected to under 37 C.F.R. §1.83(a) because of minor inconsistencies. Claims 11, 12, 14, 15, 19, 20, 22 and 23 have been amended to replace the objected terms with the terms used in the original specification. Accordingly, Applicants respectfully request that this objection be withdrawn.

Claims 10, 20, 22 and 23 are objected to under 37 C.F.R. §1.75(a) because of typographical errors. Applicants respectfully submit that this objection is now believed to be moot in view of the current amendments in the claims.

Claim 5 is rejected under 35 U.S.C. §112, second paragraph. Applicants respectfully submit that this rejection is now believed to be moot in view of the current amendments in claim 5.

In addition, the Examiner rejected claims 1-5, 9-11 and 19 under 35 U.S.C. §102(e) as being anticipated by Sakaedani et al. (U.S. Patent No., 6,064,360); and rejected claims 1-6, 8-11 and 19 under 35 U.S.C. §103(a) as being unpatentable over ARA (Applicant's Related Art) in view of Sakaedani et al. Applicant respectfully traverses these rejections.

The rejection of claims 1-5, 9-11 and 19 under 35 U.S.C. §102(e) as being anticipated by Sakaedani et al. is respectfully traversed and reconsideration is requested.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "...a capacitor connected between the ground voltage and a gate-on voltage for charging electric charge with the gate-on voltage until a time of power-off

and for applying a voltage higher than the ground voltage to the each one of the gate lines upon power-off." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 1 and claims 2-5, which depend therefrom, are allowable over the cited references.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "...accumulating electric charges using a capacitor connected to a gate-on voltage during power-on..." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicant respectfully submits that claim 9 and claim 10, which depends therefrom, are allowable over the cited references.

Claim 11 is allowable over the cited references in that claim 11 recites a combination of elements including, for example, "...an electric charge accumulator having a capacitor coupled to the output of the gate low voltage selector and the second voltage source, the capacitor is connected between a gate-on voltage source and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicant respectfully submits that claim 11 is allowable over the cited references.

Claim 19 is allowable over the cited references in that claim 19 recites a combination of elements including, for example, "...an electric charge accumulator having a capacitor coupled to the output and the second voltage source, the capacitor connected between a gate-on voltage and the second voltage source wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicant respectfully submits that claim 19 is allowable over the cited references.

The rejection of claims 1-6, 8-11 and 19 under 35 U.S.C. §103(a) as being unpatentable over ARA in view of Sakaedani et al. is respectfully traversed and reconsideration is requested. Because ARA fails to cure the deficient teaching of Sakaedani et al. as discussed above,

Applicant respectfully submits that claims 1-6, 8-11 and 19 are allowable over the cited references.

Applicants believe the application is in condition for allowance and early, favorable action is respectfully solicited. If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: February 17, 2006

Respectfully submitted,

By _____

Rebecca Goldman Rudich
Registration No.: 41,786
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorney for Applicant